

**AMENDMENTS**

***In the Claims:***

These claims replace all prior versions and listings of claims in the above-referenced application.

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- E1
- 1            1-15. (Canceled)
- 1            16. (New) An apparatus comprising:
- 2            a multiply accumulate (MAC) unit coupled to operand busses at respective
- 3 operand inputs, the MAC unit configured to latch a first multiple-bit data value during
- 4 a first cycle and execute the MAC functions on the first multiple-bit data value during
- 5 the next subsequent cycle while latching a second multiple-bit data value, the MAC
- 6 unit further configured to supply a first MAC result responsive to the first multiple-bit
- 7 data value on a result bus once the first MAC result is available and latch a second
- 8 MAC result responsive to the second multiple-bit data value;
- 9            a register coupled to the result bus and configured to latch the first MAC
- 10 result; and
- 11            a miscellaneous logic unit coupled between the result bus and the register, the
- 12 miscellaneous logic unit configured to generate first and second control signals
- 13 responsive to at least one certain exceptional condition, wherein when the first control
- 14 signal is asserted the MAC unit supplies the second MAC result on the result bus,
- 15 when the second control signal is asserted the first MAC result is driven from the
- 16 register onto the result bus, and wherein when the second control signal is not asserted
- 17 a miscellaneous-unit generated result is driven onto the result bus.
- 1            17. (New) The apparatus of claim 16, wherein the miscellaneous logic unit
- 2 is configured to identify and exceptional condition responsive to an operand.
- 1            18. (New) The apparatus of claim 16, wherein the miscellaneous logic unit
- 2 is configured to recognize an exceptional condition identified by the MAC unit.

E1 1           19.   (New) The apparatus of claim 18, wherein the miscellaneous logic unit  
2 directs the replacement of one of the first and second MAC results with a  
3 representation of the exceptional condition.

1           20.   (New) A method for performing single-instruction multiple-data  
2 instructions comprising:  
3           applying a plurality of data values on an operand bus for two consecutive  
4 cycles;  
5           latching a first data value in a multiply accumulate (MAC) unit during a first  
6 cycle;  
7           initiating execution of the multiply and accumulate functions on the first data  
8 value and latching a second data value in the MAC unit during a second cycle;  
9           deferring a first MAC unit result responsive to the first data value;  
10          initiating execution of the multiply and accumulate functions on the second  
11 data value during a cycle subsequent to the second cycle to generate a second MAC  
12 unit result; and  
13          generating a plurality of control signals responsive to the first data value, the  
14 second data value, and an exceptional condition when identified by the MAC unit.

1           21.   (New) The method of claim 20, further comprising applying the  
2 plurality of control signals to arrange a combination selected from the first MAC unit  
3 result, the second MAC unit result, and a representation of an exceptional condition.

1           22.   (New) The method of claim 20, wherein deferring comprises  
2 forwarding the first MAC unit result to a register.

1           23.   (New) The method of claim 20, wherein generating comprises  
2 determining when an operand is invalid.

1           24.   (New) The method of claim 20, wherein generating comprises  
2 determining when an operation in combination with an operand will produce an  
3 exceptional condition.

E1  
1           25.   (New) The method of claim 20, further comprising forwarding the  
2 combination to a result bus.

1           26.   (New) An apparatus comprising:  
2           means for producing a plurality of control signals responsive to a first data  
3 value, a second data value, and an exceptional condition, wherein the exception  
4 condition results from the execution of a multiply accumulate (MAC) unit over the  
5 first and second data values; and  
6           means for arranging a combination selected from a first MAC unit result, a  
7 second MAC unit result, and a representation of the exceptional condition responsive  
8 to the plurality of control signals.

1           27.   (New) The apparatus of claim 26, wherein the first MAC unit result is  
2 responsive to the first data value.

1           28.   (New) The apparatus of claim 26, wherein the second MAC unit result  
2 is responsive to the second data value.

1           29.   (New) The apparatus of claim 26, wherein the exceptional condition is  
2 identified by the MAC unit.

1           30.   (New) The apparatus of claim 26, wherein the exceptional condition is  
2 identified by the means for producing the plurality of control signals responsive to at  
3 least one of the first and second data values and an opcode.